

# Hani Ahmad

**Current Address (home):**

**102 Umm Al Qura street**

**Amman, Jordan 11937**

**Phone: +962 795 930140**

**Email: [h.ahmad@psut.edu.jo](mailto:h.ahmad@psut.edu.jo)**

---

## **PROFILE:**

- 12+ years of industry experience as systems and transistor level design engineer in Analog/RF, and Power Management IC (PMIC) using CMOS/Bipolar processes.  
Experience includes:
    - systems architecture and transistor-level design of LED drivers, SMPS Buck and Boost converters, chargers, LDOs and Switches in addition to several analog blocks (ADC/DAC, OPAMPS, Bandages, comparators, LC-tank Oscillators, DLLs, PLLs, etc.,).
    - Designing RF-front-end circuits such LNAs, Pas and Mixers.
    - Feedback architectures to meet load fast transients with digital or analog control including embedded regulators in application processors/Modems.
    - Advanced envelope tracking techniques and architectures.
    - Multi-phase embedded voltage regulators and techniques to optimize efficiency.
    - Familiarity with smartphone platforms including PMIC, RF front-end, Envelope-tracking, transceivers and overall functionality.
  - 7 years of experience in the Telecommunication industry. This includes voice networks and protocols, IP and MPLS networks in addition to SONET/WDM networks and equipment.
  - B.Sc, M.Sc and Ph.D. degrees, all in Electrical/Electronic Engineering.
- 

## **TECHNICAL SKILLS:**

- SMPS (Switch Mode Power Supplies) architectures, design and modeling. This includes non-isolated DC-DC buck and boost converters, Chargers, LDOs and switches.
- Analog and Digital Control architectures for DC-DC converters.
- Analog Circuit design and simulation using Cadence Tools (Spectre) and Pspice Blocks design include ADC/DACs, PLLS, DLLs, Bandgaps, OP-AMPs, Comparators, Ring and LC-Oscillators, etc.,
- CMOS and Bipolar technologies.
- Narrow-and and Broadband LNAs, Mixers and PAs.
- Digital design: Verilog HDL, Synopsys Design Compiler (DC), First Encounter (Automatic place and (route tool), Prime Time, Xilinx FPGAs /CPLDs, device physics, and VLSI circuits.
- Mathcad and Simulink of Matlab for system-level modeling and prototyping.
- Nanosim for mixed-signal system-level simulation.
- Languages: C, C++, JAVA, and Verilog.
- Operating Systems: MS Windows, Linux and UNIX.

---

## **WORK EXPERIENCE**

### **Princess Sumaya University of Technology (PSUT) (September 2016 - present)**

Assistant professor, Electrical Engineering department.

- Teaching and conducting research: Basic and advanced electronics classes including Analog, power management integrated circuits (PMIC), Power electronics, communication electronics and RF microelectronics (RFIC).
- Offering and Administering senior design projects.
- Creating new advanced classes to add depth to the Electronics curricula.
- Electronics engineering ABET program coordinator
- Industry-University cooperation group leader
- Electronics curricula management group leader
- Electronics CAD tools (Cadence and ADS) support.
- Patents evaluation and filing procedure seminars.

### **Qualcomm Inc. (May 2008– November 2015)**

#### **Senior Staff Design and Systems Engineer, PMIC group**

##### **Example Projects:**

- Led the work on White LED (WLED) driver utilizing Boost converter. The task included:
  - ✓ Market competitive analysis
  - ✓ System level specifications
  - ✓ System level modeling using Simulink and Cadence
  - ✓ Transistor level design of all building blocks for the WLED o Supervising layout and chip testing.
- Led the work on digitally controlled buck regulator with fast response to wide range of load transients. Specific contributions include:
  - ✓ Selecting the overall architecture based on system requirements, current load profile, speed, and components values.
  - ✓ System-level design and modeling using Matlab and Simulink.
  - ✓ Investigated and analyzed several digital pulse width modulator (DPWM) architectures and selected the one that fits best the application in hand and that satisfies the given requirements.
  - ✓ Design of several Delay locked loops as part of DPWM architecture.
  - ✓ Used Solido statistical tools to verify design across process corners (PVT).
  - ✓ Designed several flavors of switches that will be used on-chip to provide voltages to switchable loads.
  - ✓ Participated in all block design and layout reviews.
  - ✓ Led the verification team in mixed-signal simulation at the buck and chip level using mixed-signal AMS/APS/Spectre Cadence simulation environment.
  - ✓ Participated in post-silicon characterization and provided feedback for metal-1 tape-out
- Designed low voltage, high voltage, HDMI and OTG types of switches.
- Helped in designing several circuits in SMPS-based battery chargers.

- Helped in designing several Low Dropout Regulators (LDOs).
- System-level architecture including control loops for the multi-phase embedded regulator.

## **Linear Technology (May 06- May 08)**

### **Analog Design Engineer: Power Management Group**

- Designed LED Driver ICs using high voltage Bipolar process. Typical design flow includes the following:
  - ✓ Generation of one-page product definition.
  - ✓ Generation of objective specs document that includes electrical characteristics, possible applications, and brief competitor analysis.
  - ✓ Design of average model for the buck and the PWM modulator to be used in the AC simulations.
  - ✓ Compensation design to stabilize the control loop.
  - ✓ Selection of power stage, inductors and capacitors
  - ✓ Design of startup circuitry that includes band gap core, current limit and internal LDO.
  - ✓ Design of 1 MHz oscillator (or 2 MHz with metal option), Driver, Error Amp, and Current Sense circuits.
  - ✓ Work with and guide mask designers into the layout using standard Cadence tools.
  - ✓ Design and layout reviews for the overall IC.

## **Intel Corporation (May 05- May 06)**

### **Design Engineer Intern: Power Management Group**

- ✓ Participated in the system-level definition of the multi-phase buck converter
- ✓ System-level modeling and simulation using Simulink and cadence primitive elements
- ✓ Designed several current sensing schemes.
- ✓ System level simulation using Nanosim.
- ✓ Test bench construction to apply different types of Sims such as aging Sims and extraction.
- ✓ Helped in generating different testing and design documents.

## **Ciena Corporation (May 2002-May 2004)**

### **Lead Systems Engineer: System Architecture and Development Group.**

- Specified requirements for the "Control Plane" that allowed service auto-provisioning across Ciena products (Metro products and CorDirector) and between Ciena products and third-party equipment. This includes specifying the interfaces, signaling, routing and neighbor discovery protocols.
- Specified DCN (Data Communication Network) requirements for Ciena products. This task included a detailed set of requirements for IP and OSI protocol stacks to allow for seamless communication among Ciena's equipment and between Ciena and third-party equipment.
- Designed specifications and delivered requirements on time for several Line Cards (Circuit Packs). These modules include electrical tributary cards (such as E1, E3 and DS3), SONET/SDH cards such as OC3 and STM1 and SAN cards such as ESCON and FC. For each module, specified Functional Blocks, Performance Monitoring, Defects, Failure, Alarms, Test Access, Silent Failure, PRBS, Loopbacks, Cross-connection

**Cisco Systems, Inc.** (Jan 2000-May 2002)

**Lead Design Engineer: Global Center of Expertise (GCoE).**

- Evaluated and performed reliability analysis on core network design for several service providers. These networks were IP and/or ATM MPLS/VPN-based. The main network elements used in these networks were Cisco GSR, MGX, BPX, 7200, 3600, 2500 series and other vendor equipment.
- Designed and defined architectures for several national and international service providers' networks. In these assignments field trials were conducted at the customer site, and system configuration and on-site training are also offered to the clients.
- Taught and supervised Routing Protocols (RIP, OSPF, and BGP) Boot-camps to internal groups within Cisco.

**Telcordia Technologies /Bellcore** (May 1997- Jan 2000)

**Sr. Systems Engineer:** Navisink Research and Engineering Center.

- Led a team in defining a next-generation architecture for Trunk Gateway GR (Generic Requirements) for voice-over IP.
- Provided on-site and off-site consulting for several national and international service providers. These consulting assignments included network design and architecture, Capacity planning, Migration strategies, Strategic Planning, Capital expenditure and signaling (SS7 and PNNI).
- Designed and assessed several SONET network architectures and protection schemes for national and international service providers. Using this assessment as a guide, these service providers were able to pick the appropriate architecture that serves their specific current and future needs.
- Represented 3 RBOCS clients in the ATM Forum, ITU, and T1S1 standard bodies. The main contributions were in Broadband signaling, services and architecture.
- Designed and produced the content for a free web portal called "Consultant on Line" to help medium to large enterprise businesses define their telecom needs.
- Wrote many technical papers (Special Reports) on topics of interest to Telcordia customers. These include: Next generation network architecture alternatives (using ATM, IP, SONET, DWDM and MPLS technologies), Migration of traditional ILECs networks to a multi-service platform, Technical Comparison between Voice over ATM (using AAL2, AAL1, AAL5) and Voice over IP, How to Select and obtain an ATM addressing scheme.

## EDUCATION:

- **MBA**, W.P.Carey, Arizona State University, 2011
  - **Ph.D.** (EE), Arizona State University, Ira. A. Fulton School of Engineering, 2009
  - **Professional Certification in Telecommunications**, Columbia University, NY, NY.
  - **Analog Designer** (Professional Sequence), UC Berkeley, Berkeley, CA
  - **VLSI Design Engineering Certification**, UC Santa Cruz, Santa Cruz, CA
  - **Unix Administrator Certification**, Kean University, Union, NJ
  - **M.Sc.** Electrical Engineering (CIE), STEVENS Institute of Technology, Hoboken, NJ.
  - **M.Sc.** Computer Science, STEVENS Institute of Technology, Hoboken, NJ.
  - **B.Sc.**, Electrical Engineering University of Jordan, Jordan.
- 

## SELECTED PUBLICATIONS AND GRANTED PATENTS:

Ibrahim Abuishmais, Fadi R. Shahroury, **Hani Ahmad**, "A Design Methodology of High-Efficiency Dimmable Current Sink for Current-Regulated Drivers", Electronics Journal, August 2022.

Khaldoon Abugharbieh, Basel Yaseen, Abdullah Deeb, **Hani Ahmad**, Ayman Jeit, "A Fully Integrated Mixed-Mode LDO Regulator with Fast Transient Response, Journal of Circuits, Systems, and Computers. July 2022 (<https://doi.org/10.1142/S0218126622503005>)

Abdulhadi, Osama & Zetawi, Alaa & Shahroury, Fadi & **Ahmad, Hani** & Akour, Amneh. (2022), Design and Implementation of Rapid Shutdown Filters for Roof Integrated Photovoltaic Cells", International journal of simulation: systems, science & technology. 10.5013/IJSSST.a.23.01.10.

Jaradat, Raya & Shahroury, Fadi & **Ahmad, Hani** & Abuishmais, Ibrahim. (2022), "DESIGN METHODOLOGY FOR NARROW-BAND LOW NOISE AMPLIFIER USING CMOS 0.18  $\mu\text{m}$  TECHNOLOGY", Jordanian Journal of Computers and Information Technology. 8. 1. 10.5455/jcit.71-1637577305.

Shahroury, Fadi & **Ahmad, Hani** & Abuishmais, Ibrahim. (2022), "Design Aspects of a Single-Output Multi-String WLED Driver Using 40 nm CMOS Technology", Journal of Low Power Electronics and Applications. 12. 5. 10.3390/jlpea12010005.

Zetawi, Eng & Abdulhadi, Eng & Shahroury, Fadi & **Ahmad, Hani** & Akour, Amneh. (2021), "Components and Specification of Rapid Shutdown for Roof PV Systems". 182-185. 10.1109/ICM52667.2021.9664910.

**Ahmad, Hani** & Shahroury, Fadi & Abuishmais, Ibrahim. (2021), "A Multi-Output Multi-String High-Efficiency WLED Driver Using 40 nm CMOS Technology", Journal of Low Power Electronics and Applications. 11. 47. 10.3390/jlpea11040047.

**Ahmad, Hani** & Shahroury, Fadi. (2020), "Design of a High Efficiency WLED Driver in 40 nm CMOS Technology", 1-4. 10.1109/ICM50269.2020.9331783.

**Ahmad, Hani** & Gammoh, Nour & Bader, Mariana. (2020), "Essential Features/Issues of a Multi-Phase Switching Synchronous Buck Regulator", Advances in Science, Technology and Engineering Systems Journal. 5. 1056-1059. 10.25046/aj0505130.

Gammoh, Nour & Bader, Mariana & **Ahmad, Hani**. (2019), "Design and Simulation of a Three-Phase Switching Synchronous Buck Regulator", 1-7. 10.1109/PEDS44367.2019.8998899.

Mustafa Keskin, **Hani Ahmad-Assi**, Paul Brian Sheehy, Robert Philip Gilmore, "Faster battery charging in consumer electronic devices" **US patent number 9,819,206**, November 17, 2017

**Ahmad, Hani** & Bakkaloglu, Bertan. (2010), "A digitally controlled DC-DC buck converter using frequency domain ADCs", 1871 - 1874. 10.1109/APEC.2010.5433488.

**Ahmad, Hani** & Bakkaloglu, Bertan. (2010), "A 300mA 14mV-ripple digitally controlled buck converter using frequency domain  $\Delta\Sigma$  ADC and hybrid PWM generator", 53. 202 - 203. 10.1109/ISSCC.2010.5433985.

**Ahmad, Hani** & Bakkaloglu, Bertan. (2008), "A DC-DC digitally controlled buck regulator utilizing first-order  $\Sigma$ - $\Delta$  frequency discriminators", 346 - 352. 10.1109/APEC.2008.4522745.

**Ahmad, Hani** & Bakkaloglu, Bertan. (2008), "A DC-DC digitally controlled buck regulator utilizing multi-bit  $\Sigma$ - $\Delta$  frequency discriminators", Conference Proceedings - IEEE Applied Power Electronics Conference and Exposition - APEC. 1543-1548. 10.1109/APEC.2008.4522930.

Poornachandran, R. & **Ahmad, Hani** & Cam, Hasan. (2005), "Energy-efficient task scheduling for wireless sensor nodes with multiple sensing units. PCCC 2005. 24th IEEE International Performance, Computing, and Communications Conference, 2005.409 - 414.